## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

## SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 9-13, page 8 lines 6-9 and FIG. 1, as originally filed. Thus, no new matter has been added.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-21 under 35 U.S.C. §102(e) as being anticipated by Rezek et al. '256 (hereafter Rezek) has been obviated in part, is respectfully traversed in part, and should be withdrawn.

Rezek concerns a method and apparatus for optimizing a circuit design having multi-paths therein (Title).

Claim 1 provides a step for **analyzing a netlist** of a circuit design to identify **a plurality of sources** for a plurality of clock signals. In contrast, Rezek appears to be silent regarding a step of analyzing a netlist of a circuit design. Furthermore, Rezek appears to be silent than any such analysis identifies sources for the clock signals. In particular, FIG. 3 of Rezek appears to contemplate that the clock signals are received from a clock definition file 54, not from an analysis of a netlist.

Therefore, Rezek does not appear to disclose or suggest a step for analyzing a netlist of a circuit design to identify a plurality of sources for a plurality of clock signals as presently claimed. Claims 14, 20 and 21 provide similar language.

Claim 1 further provides a step for determining a plurality of **relationships among** the clock signals. Despite the assertion in the Office Action, Rezek appears to be silent regarding a standard (logic) optimizer 50 (allegedly anticipating the claimed method steps) generating any relationships among the clock signals. In particular, the text of Rezek cited in the Office Action only appears to discuss which clock signals are used by each state device. Rezek appears to say nothing about relationships among the clock signals themselves. Therefore, Rezek does not appear to disclose or suggest a step for determining a plurality of relationships among the clock signals as presently claimed. Claim 20 provides similar language.

Claim 1 further provides a step for **performing a structural analysis** based on (i) the clock signals and (ii) the relationships to generate the timing constraints for the circuit design. In contrast, Rezek appears to be silent regarding performance of a structural analysis based on some unidentified relationships among the clocks. Furthermore, the timing constraints generated by Rezek appear to be based on optimization parameters. The optimization parameters appear to be based on timing analysis results. Finally, the timing analysis results

appear to be based on timing models 58 (for example, see Rezek, column 9, line 61-column 10, line 5). Nothing in Rezek appears to mention that the timing constraints are based on both the clock signals and the unidentified relationships among the clock signals. No evidence is provided in the Office Action that the unidentified relationships are somehow allegedly inherent to the timing models 58 or any of the steps leading up to the timing constraints. Therefore, Rezek does not appear to disclose or suggest a step for performing a structural analysis based on (i) the clock signals and (ii) the relationships to generate the timing constraints for the circuit design as presently claimed. Claim 20 provides similar language. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 14 further provides a step for **querying a user** for a plurality of parameters for the clock signals. Despite the assertion in the Office Action, Rezek appears to be silent regarding querying a user for clock signal parameters. In particular, the only user-provided parameters in Rezek appear to be optimization parameters per column 10, lines 19-27. Therefore, Rezek does not appear to disclose or suggest a step for querying a user for a plurality of parameters for the clock signals as presently claimed.

Claim 14 further provides a step for **performing a structural analysis** based on (i) the clock signals and (ii) the (user-queried) parameters to generate the timing constraints for

the circuit design. In contrast, Rezek appears to be silent regarding a structural analysis based on some unidentified user-queried parameters for the clock signals. In particular, the timing constraints generated by Rezek appear to be based on optimization parameters. The optimization parameters appear to be based on timing analysis results. Finally, the timing analysis results appear to be based on timing models 58 (for example, see Rezek, column 9, line 61-column 10, line 5). Nothing in Rezek appears to mention that the timing constraints are based on both the clock signals and user-queried parameters for the clock signals. Therefore, Rezek does not appear to disclose or suggest a step for performing a structural analysis based on (i) the clock signals and (ii) the parameters to generate the timing constraints for the circuit design as presently claimed. Claim 21 provides similar language. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2, 6 and 12 provide test clock signals. Despite the assertions in the Office Action, Rezek appears to be silent regarding test clock signals. In particular, the only "test" elements mentioned by Rezek appears to be "test vectors" in column 11, line 36. Therefore, Rezek does not appear to disclose or suggest test clock signals as presently claimed. As such, claims 2, 6 and 12 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 3, 4 and 7 provide steps for **eliminating timing constraints**. Despite the assertion in the Office Action, Rezek appears to be silent regarding the elimination of any timing constraints. In particular, the only "elimination" mentioned by Rezek appears to be an elimination of redundant logic in column 10, line 23. The text of Rezek cited in the Office Action only appears to discuss **adding timing constraints**. Therefore, Rezek does not appear to disclose or suggest eliminating timing constraints as presently claimed. As such, claim 3, 4 and 7 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 8-12 and 15 provide steps for generating/determining **specific relationships among the clock signals.** As mentioned above in the arguments for claim 1, Rezek appears to be silent regarding the standard (logic) optimizer 50 (allegedly anticipating the claimed method steps) generating any relationships among the clock signals. Therefore, Rezek does not appear to disclose or suggest generating relationships among the clock signals as presently claimed. As such, claims 8-12 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 16 and 17 provide steps for **querying a user** for specific parameters of the clock signals. As mentioned above in the arguments for claim 14, the only user-provided parameters in Rezek appear to be optimization parameters per column 10, lines 19-27. Rezek appears to be silent regarding user-queried parameters

for the clock signals. Therefore, Rezek does not appear to disclose or suggest steps for querying a user for parameters of the clock signals as presently claimed. As such, claims 16 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5, 18 and 19 depend from independent claims 1 and 14, which are now believed to be allowable. As such, claims 5, 18 and 19 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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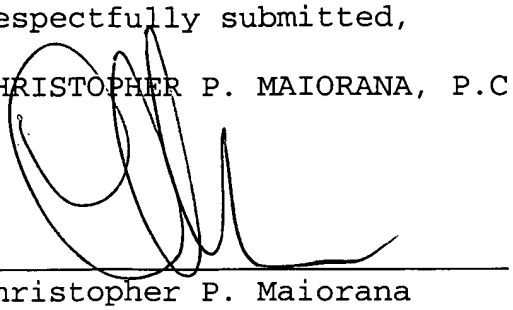

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